Remarks

Claims 1-3 are pending and under consideration.

In the Office Action of July 31, 2002, claims 1-3 were rejected as being anticipated by *Yamazaki, et al. (US 6,246,070)*. In response, claim 1 has been amended.

Claim 1 now recites that the resultant transistor is free of etch mask structures. As is clearly shown in Fig. 3 of *Yamazaki*, etch mask structures 109 and 112 remain in the resultant device. Further, claim 1 recites the inclusion of an electrode containing series of layers that is provided over the protection layer.

As discussed at page 12 of the present application, the LDD or source-drain region is formed by doping through the protective layer 8 and an etching process is avoided. This provides an improvement in productivity in the production of the TFT devices. Additionally, since the polysilicon film 7 is not etched unnecessarily, unwanted breakdown voltages can be avoided.

It is submitted that there is no fair disclosure or suggestion in *Yamazaki* to remove these structures as is shown, e.g, in Fig. 1 of the present application.

Accordingly, it is submitted that claim 1 and, a fortiori, claim 2-3 are patentable over *Yamazaki*.

In view of the forgoing, it is submitted that the application is in condition for allowance. Notice to that effect is requested.

Respectfully submitted,

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I hereby certify that this document and any being referred to as attached or enclosed is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, Washington, D.C. 20231, on

12/31/02 JoEllen Hogan
Date

APPENDIX

VERSION WITH MARKINGS SHOWING CHANGES MADE

IN THE CLAIMS:

Please amend claim 1 to read as follows:

1. (Amended) A bottom-gate thin-film transistor comprising a gate electrode, a gate insulating film, an active layer, and a protective insulating film deposited in that order on a substrate~~,~~; and

various layers formed over said protective film with at least one electrode extending therethrough that is operatively and electrically connected to said active layer, LDD region or source-drain region;

wherein,

the protective insulating film has a thickness of 100 nm or less, and the protective insulating film is formed on any one of the active layer, an LDD region, and a source-drain region~~.~~, and

there is no etched mask structure within the thin-film transistor structure.